WEST

Generate Collection Print

L5: Entry 5 of 12 File: TDBD Dec 1, 1988

TDB-ACC-NO: NN8812470

DISCLOSURE TITLE: Automotive Engine Analyzer High Speed Data Card

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, December 1988, US

VOLUME NUMBER: 31
ISSUE NUMBER: 7
PAGE NUMBER: 470 - 473

PUBLICATION-DATE: December 1, 1988 (19881201)

CROSS REFERENCE: 0018-8689-31-7-470

DISCLOSURE TEXT:

- This article describes a high speed data card (HSDC) for an automotive engine analyzer which measures the period between adjacent flywheel teeth pulses and saves the result in a memory buffer. It serves as an interface between the flywheel gear and a personal computer (PC). ***** SEE ORIGINAL DOCUMENT ***** The basic function of the HSDC is to measure the period between adjacent flywheel teeth pulses and save the result in a memory buffer. For a flywheel gear with 150 teeth the HSDC saves 150 words (16 bits each) every crankshaft revolution. The engine analyzer main processor reads this data every crankshaft revolution and saves it in its main memory. The data is later correlated and processed with other engine data for engine performance analysis. The HSDC is an integral part of the engine analyzer and consists of an HSDC processor and interface, a dual random-access memory (RAM) buffer and PC bus interface. Fig. 1 is a high level block diagram of the HSDC. The HSDC processor is based on Intel's* 8052 single chip microcontroller. The 8052 has all the following features onboard: (a) 8 bit CPU (b) 8K bytes of ROM (c) 256 bytes of RAM (d) 32 I/O lines (e) Three 16-bit timers/counters (f) Five source interrupt structure with two priority levels (g) Full duplex serial port (h) Boolean processor The HSDC processor performs the flywheel data measurement using two 16-bit internal counters. In addition, it arbitrates access control of the dual memory buffer between it and the main processor. Fig. 1 shows the connectivity of the 8052 to the flywheel signal for flywheel data measurements. The flywheel signal is divided by 2. The ***** SEE ORIGINAL DOCUMENT ***** output signal and its complement feed the external interrupt inputs (INT0 and INT1) of the 8052. Fig. 2 shows the flywheel signal with the interrupt inputs. The 8052 is configured in a special mode where -INTX (INT0 and INT1) inputs enable TIMER X (timer0 and timer1). Fig. 3 depicts the circuit within the 8052 gating the timers with the external interrupts. The timers are set up to operate as counters (bit C/-T =1); allowing it to count the external input clock (Ext Clk). Timer0 and timer1 operate on a 4 MHz external clock. The TRX and gate bits are set in software, enabling the counters when the corresponding interrupt input is high. With the interrupts programmed in the edge-triggered (high to low transition) mode, the 8052 is prompted to save the value of the corresponding counter in memory when the interrupt line is active. That is, during INT0, TIMER 0 value is saved in memory before clearing the timer and getting it ready for the next cycle. For example, consider a flywheel gear with 150 teeth and running at 2000 rpm. The value in the timer on interrupt will be: (4000000 counts/sec) / (2000 rev/min x150 teeth/rev x 1min/60 sec.) = 800 The top dead center (TDC) signal is also an interrupt input to the 8052. On every TDC signal the 8052 switches the memory access control signal between RAM bank0 and bank1. For example, if the 8052 has access to bank1 and the main processor has access to bank0, on the next TDC this access control is switched. The 8052 performs other tasks including Power-On Self Text (POST), handshaking with the main processor for configuration parameters and error

control, and background diagnostics. Fig. 4 is a functional flow chart illustrating the major tasks of the HSDC processor. The dual RAM buffer consists of bank0 and bank1. Each bank consists of two 8K x 9 static memory modules. This arrangement allows for either memory transfers with the main processor or 8-bit transfers with the 8052. The ninth bit is used as a parity bit for data integrity. The transceivers (XCVRS) shown in Fig. 1 perform the added function of parity generation on memory writes and parity checking on memory reads. In case of parity error, the parity logic block latches the error and informs the corresponding processor which will later reset the error latch. Access to a memory bank is multiplexed between the 8052 and the main processor using address multiplexers. The multiplexing control is generated by the 8052 and toggled every TDC. The PC interface consists of buffers, address latches, and address decode and read/write logic specific to the Micro Channel** bus. * Trademark of Intel Corp. ** Trademark of IBM Corp.

SECURITY: Use, copying and distribution of this data is subject to the restictions in the Agreement For IBM TDB Database and Related Computer Databases. Unpublished - all rights reserved under the Copyright Laws of the United States. Contains confidential commercial information of IBM exempt from FOIA disclosure per 5 U.S.C. 552(b)(4) and protected under the Trade Secrets Act, 18 U.S.C. 1905.

COPYRIGHT STATEMENT: The text of this article is Copyrighted (c) IBM Corporation 1988. All rights reserved.

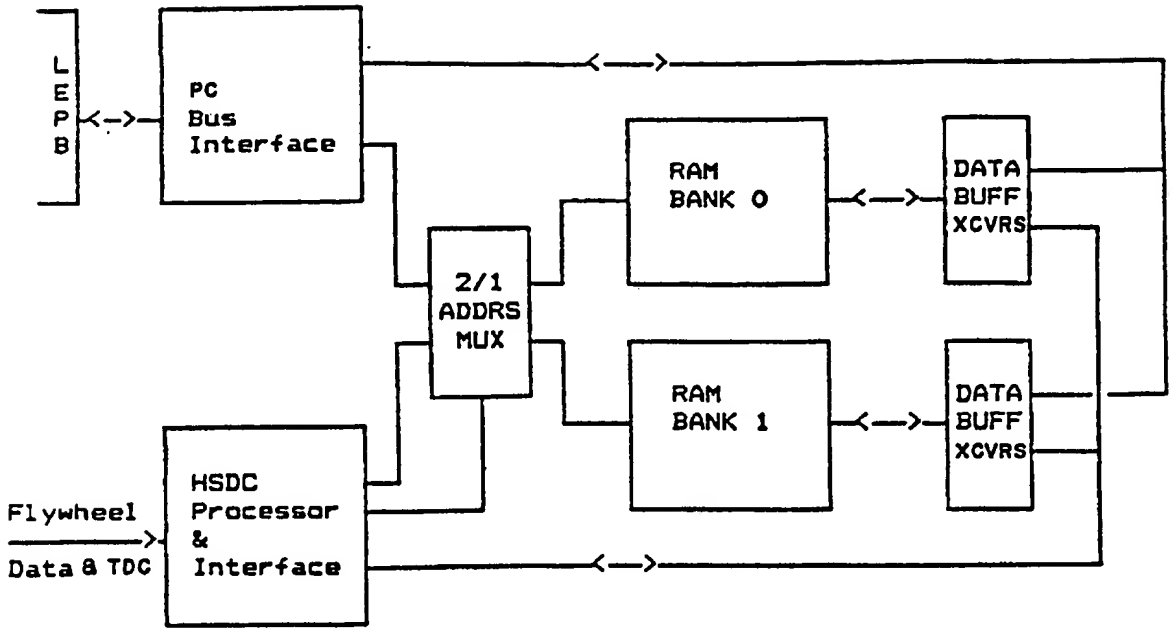

FIG. 1

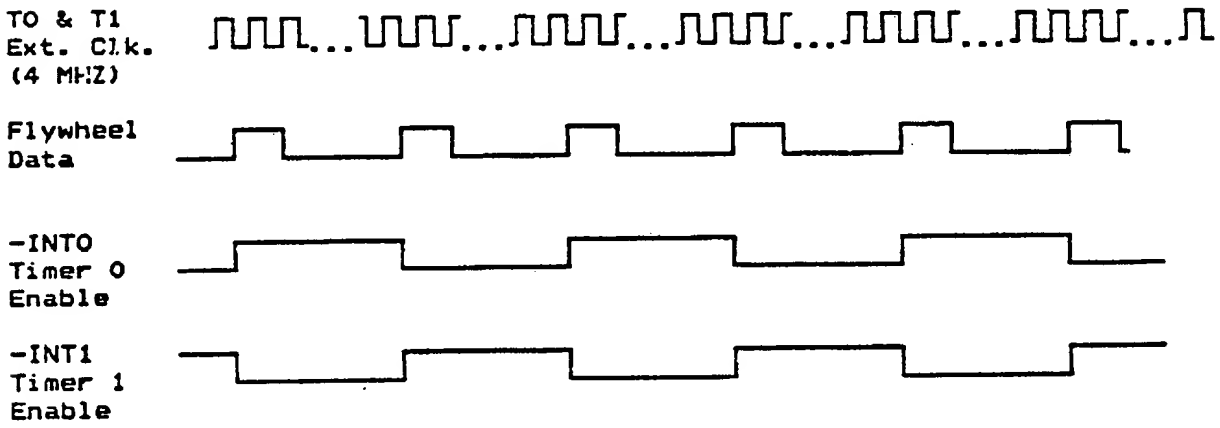

FIG. 2

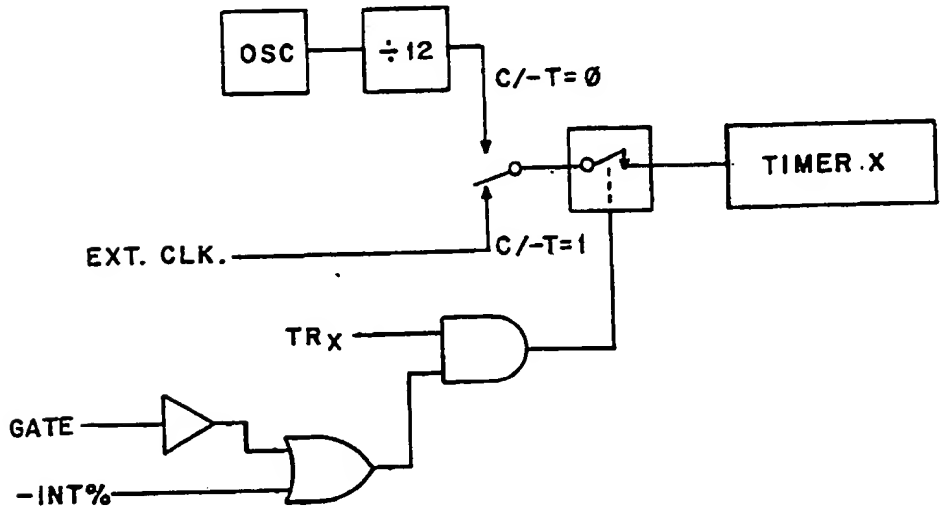

FIG. 3